[0070] FIGS. 1 to 3 are schematic views illustrating a conventional method for fabricating a semiconductor device. Referring to FIG. 1, after a ~~film is deposited on a wafer 10~~ deposition process by the CVD apparatus is completed, the ~~deposited~~ layer 20, such as an oxide layer, ~~exhibits a tendency to have a higher growth rate at a dead zone region 24 (see FIG. 2) corresponding to an upper sidewall or edge portion~~ is deposited on the upper sidewall of the wafer 10 as well as on the whole front surface of the wafer 10[[,]] due to the characteristics of the gas flow used to form the layer.

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Please replace paragraph [0075] with the following amended paragraph:

[0075] Thereafter, as shown in FIG. 2, ~~a~~ when the conventional CMP process is performed ~~to planarize~~ on the deposited layer 20, the layer 20 on the front surface of the wafer 10 is planarized with a uniform thickness. ~~Note that the planarized deposited layer 22 of the upper surface side has a uniform thickness extending nearly to the edge of the wafer, but the planarized deposited layer in the dead zone region 24, corresponding to the upper sidewall portion of the wafer 10, has a non-uniform thickness due to the inherent restrictions of the CMP process and the initial gas flow characteristics. As a result, the deposited layer on the upper side wall portion of the wafer 10 remains thicker relative to the planarized deposited layer 22 remaining on the upper surface of the wafer 10.~~ However, the layer 20 on the upper sidewall 24 of the wafer 10 including an edge line of the wafer that is hereinafter referred to as dead zone region cannot be planarized due to the inherent restrictions of the CMP process and the initial gas flow characteristics. As a result, the layer on the dead zone region 24 remains thicker relative to the layer remaining on the front surface of the wafer 10, so that the thickness of the layer 10 is uniform on the front surface of the wafer 10 and is not uniform over the dead zone region 24. Moreover, the slurries may accumulate ~~at~~ on the dead zone region 24 and thus the probability of particle occurrence becomes higher. As can be seen, after the CMP process is completed, the difference in the thickness of the deposited layer 20 between

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the uniform planarized deposited layer 22 and the non-uniform portion at the dead zone region 24 is increased relative to the pre-planarized conditions.

Please replace paragraph [0080] with the following amended paragraph:

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[0080] Afterwards, in order to form a pattern on the planarized deposit layer, a photolithography process and a dry etch process are sequentially performed. In the general patterning process, the layer 20 coated on an edge portion of the front surface of the wafer 10 is removed through an edge expose wafer (EEW) process ~~is also performed to remove the deposited layer of the exposed sidewall of the wafer 10~~.

Please replace paragraph [0085] with the following amended paragraph:

A5

[0085] ~~Referring to~~ However, as shown in FIG. 3, ~~since~~ the deposited layer 20 ~~in~~ coated on the dead zone region 24 ~~was thicker than that of the planarized deposited layer 22~~, cannot be removed even after the CMP and etching processes[[,]] since the layer 20 on the dead zone region 24 is thicker than the layer 20 on the front surface of the wafer 10, so that a residual oxide 26 still remains ~~at the upper sidewall portion of the wafer 10~~ on the dead zone region. This is because the dry etch is performed with reference only to the thickness of the planarized deposited layer 22 formed on the upper surface of the wafer 10.

Please replace paragraph [0090] with the following amended paragraph:

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[0090] Moreover, a group of cone shaped particles 28 are generated at a boundary between the removed portion of the deposited layer and the remaining portion of the deposited layer ~~at an edge of the upper surface of the wafer 10~~ on the dead zone region. The group of cone shaped particles 28 comprise a silicon substance, such as silicon (Si), silicon dioxide (SiO_2), or the like.

Please replace paragraph [0110] with the following amended paragraph:

[0110] To achieve the above objects and other advantages, there is provided a method for fabricating a semiconductor device, including depositing a layer on a wafer and then planarizing the deposited layer. ~~The resulting planarized layer has a uniform region of uniform thickness extending along a wafer surface and nearly to an edge of the wafer, and a non-uniform region of non-uniform thickness corresponding to the edge of the wafer. A photoresist layer is coated on the planarized layer, and then a portion of the coated photoresist layer corresponding to an edge region of the wafer is removed, thereby exposing at least the non-uniform region of the planarized layer.~~ The resulting planarized layer has a uniform region of uniform thickness extending along a wafer surface, and a non-uniform region of non-uniform thickness corresponding to an upper sidewall of the wafer. A photoresist layer is coated on the planarized layer, and then a portion of the photoresist layer coated on an edge portion of the uniform region of the planarized layer and on the non-uniform region of the planarized layer is removed, thereby exposing at least the non-uniform region of the planarized layer. The exposed non-uniform region of the planarized layer is etched, and a remaining portion of the coated photoresist layer on the planarized layer is stripped, thereby forming a pattern layer comprising a portion of the uniform region of the planarized layer.

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Please replace paragraph [0115] with the following amended paragraph:

[0115] According to another aspect of the present invention, there is provided a method of fabricating a semiconductor device, including depositing a layer on a wafer, ~~with the deposited layer having a uniform region of uniform thickness extending along a wafer surface and nearly to an edge of the wafer, and a non-uniform region of non-uniform thickness corresponding to the edge of the wafer. A photoresist layer is first coated on the deposited layer, and then a portion of the coated photoresist layer is removed, corresponding to an edge region of the wafer, thereby exposing at least the non-uniform~~

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~~region of the deposited layer.~~ with the deposited layer having a uniform region of uniform thickness extending along a wafer surface, and a non-uniform region of non-uniform thickness corresponding to an upper sidewall of the wafer. A photoresist layer is first coated on the deposited layer, and then a portion of the photoresist layer coated on an edge portion of the uniform region of the deposited layer and on the non-uniform region of the deposited layer is removed, thereby exposing at least the non-uniform region of the deposited layer. At least the exposed non-uniform region of the deposited layer is etched, and then the coated photoresist layer remaining on the wafer is stripped. The uniform region of the deposited layer is then planarized to thereby form a pattern layer.

Please replace paragraph [0165] with the following amended paragraph:

[0165] ~~Referring to FIGS. 4 and 5, a deposited layer 20 is formed on a wafer 10. Note that the deposited layer 20 has a region of uniform thickness 20a extending along the wafer surface and nearly to the edge of the wafer 10, and a region 20b of non-uniform thickness corresponding to an upper sidewall or edge of the wafer 10. Thereafter, a photoresist film 30 is coated on the entire deposited layer 20 with a thickness in the range of approximately 5000-15000 Å. Afterwards, an edge portion of the photoresist film 30 is removed by an edge expose wafer (EEW) process, to thereby expose at least the edge portion of the deposited layer 20 (i.e., non-uniform region 20b) as shown in FIG. 5. As also shown in FIG. 5~~ Referring to FIGS. 4 and 5, a deposited layer 20 is formed on a wafer 10. Note that the deposited layer 20 has a region of uniform thickness 20a extending along the water surface, and a region 20b of non-uniform thickness corresponding to an upper sidewall or edge of the wafer 10. Thereafter, a photoresist film 30 is coated on the entire deposited layer 20 with a thickness in the range of approximately 5000-15000Å. That is, the photoresist film 30 is coated on the region of uniform thickness 20a and the region of non-uniform thickness 20b of the deposited

layer 20. Afterwards, a portion of the photoresist film 30 coated on an edge portion of the region of uniform thickness 20a and the region of non-uniform thickness 20b is removed by an edge expose wafer (EEW) process, to thereby expose at least the region of non-uniform thickness 20b as shown in FIG. 5, depending on the desired pattern, a portion of the uniform region 20a may also be exposed when the photoresist film 30 is removed.

Please replace paragraph [0170] with the following amended paragraph:

[0170] ~~Referring to FIG. 6, any exposed portions of the deposited layer 20, and including at least the edge portion, are removed by a subsequent conventional wet etch process. Here, the exposed non-uniform region 20b of the deposited layer 20 at the edge of the wafer 10 corresponds to the dead zone region 24 described above with reference to FIG. 2.~~ Referring to FIG. 6, any exposed portions of the deposited layer 20 including at least the non-uniform region 20b, are removed by a subsequent conventional wet etch process. Here, the exposed non-uniform region 20b of the deposited layer 20 at the sidewall of the wafer 10 corresponds to the dead zone region 24 described above with reference to FIG. 2. This exposed non-uniform region 20b is thus removed prior to performing the CMP planarization process. As a result, only a deposit layer pattern 40 (corresponding to all or a portion of the uniform region 20a) remains on the upper surface of the wafer 10. Here, a target thickness of the deposit layer removed by the wet etch process is in a range of approximately 5000-15000 Å.

Please replace paragraph [0185] with the following amended paragraph:

[0185] Referring to FIG. 8, a deposited layer 20 is formed on a wafer 10. Thereafter, the deposited layer 20 is planarized and polished using a CMP process, thereby forming a planarized layer 50 as shown in FIG. 9. Note that the planarized layer 50 has a region of uniform thickness 50a extending along the wafer surface ~~and nearly to the edge of the wafer 10~~, and a region 50b of non-uniform thickness corresponding to an upper sidewall

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or edge of the wafer 10. In the planarized layer 50, the uniform region 50a is thinner than the non-uniform region 50b.

Please replace paragraph [0190] with the following amended paragraph:

[0190] ~~Referring to FIG. 10, a photoresist film 30 is then coated on the entire planarized layer 50 with a thickness in the range of approximately 5000-15000 Å. Afterwards, an edge portion of the photoresist film 30 is removed by an edge expose wafer (EEW) process, to thereby expose at least the edge portion of the planarized layer 50 (i.e., non-uniform region 50b).~~ Referring to FIG. 10, a photoresist film 30 is then coated on the entire planarized layer 50 with a thickness in the range of approximately 5000-15000Å. That is, the photoresist film 30 is coated on the region of uniform thickness 50a and the region of non-uniform thickness 50b of the planarized layer 50. Afterwards, a portion of the photoresist film 30 coated on an edge portion of the region of uniform thickness 50a and the region of non-uniform thickness 50b is removed by an edge expose wafer (EEW) process, to thereby expose at least the region of non-uniform thickness 50b. Depending on the desired pattern, a portion of the uniform region 50a may also be exposed when the photoresist film 30 is removed.

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Please replace paragraph [0195] with the following amended paragraph:

[0195] ~~Any exposed portions of the planarized layer 50, and including at least the edge portion, are removed by a subsequent conventional wet etch process. Here, the exposed non-uniform region 50b of the planarized layer 50 at the edge of the wafer 10 corresponds to the dead zone region 24 described above with reference to FIG. 2.~~ Any exposed portions of the planarized layer 50 included at least the non-uniform region 50b are removed by a subsequent conventional wet etch process. Here, the exposed non-uniform region 50b of the planarized layer 50 at the sidewall of the wafer 10 corresponds to the dead zone region 24 described above with reference to

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FIG. 2. This exposed non-uniform region 50b is thus removed after performing the CMP planarization process. Here, a target thickness of the planarized layer removed by the wet etch process is in a range of approximately 5000-15000 Å.